

What is claimed is:

1 1. A test device for detecting alignment of deep
2 trench capacitors and word lines in DRAM devices, wherein
3 the test device is disposed in a scribe line region of a
4 wafer, the scribe line region having a plurality of pairs
5 of memory cells, each having two deep trench capacitors
6 deposited at two ends of an active area, two word lines
7 disposed above the active area, and a bit line contact
8 disposed between the two word lines and electrically
9 coupled to the active area, the test device comprising:

10 parallel first and second bar-type deep trenches
11 capacitors disposed in the scribe line region;
12 wherein the first and second bar-type deep
13 trenches capacitors extend to the first and
14 second pairs of memory cells adjacent to the
15 first active area respectively, and are
16 electrically coupled to bit line contacts of
17 the first and second pairs of memory cells
18 respectively;

19 a first transistor having a source coupled to the
20 first bar-type deep trench capacitor;

21 a second transistor having a source coupled to the
22 second bar-type deep trench capacitor; and

23 a first bit line contact electrically coupled to
24 drains of the first and second transistors.

1 2. The test device as claimed in claim 1, wherein
2 two word lines are disposed on two sides of the first bit

3 line contact respectively, as gates of the first and the
4 second transistors respectively.

1 3. The test device as claimed in claim 2, wherein
2 a first resistance between the first bit line contact and
3 the bit line contact of the first pair of memory cells is
4 detected by turning on the first transistor, and a second
5 resistance between the second bit line contact and the
6 bit line contact of the second pair of memory cells is
7 detected by turning on the second transistor.

1 4. A semiconductor device with a test device,
2 comprising:

3 a substrate having a least one scribe line region
4 and a memory region, wherein the scribe line
5 region and the memory region both have a
6 plurality of pairs of memory cells, each
7 including:

8 an active area;

9 two deep trench capacitors deposited at two ends
10 of the active area;

11 two word lines disposed above the active area;

12 and

13 a bit line contact disposed between the two
14 word lines and electrically coupled to the
15 active area; and

16 a test device disposed in the scribe line region,
17 comprising:

18 parallel first and second bar-type deep
19 trenches capacitors disposed in the scribe
20 line region; wherein the first and second

21 bar-type deep trenches capacitors extend
22 to the first and second pairs of memory
23 cells adjacent to the first active area
24 respectively, and electrically coupled to
25 bit line contacts of the first and second
26 pairs of memory cells respectively;
27 a first transistor having a source coupled to
28 the first bar-type deep trench capacitor;
29 a second transistor having a source coupled to
30 the second bar-type deep trench capacitor;
31 and
32 a first bit line contact electrically coupled
33 to drains of the first and second
34 transistors.

1 5. The semiconductor device as claimed in claim 4,
2 wherein two word lines are disposed on two sides of the
3 first bit line contact respectively, as gates of the
4 first and the second transistors respectively.

1 6. The semiconductor device as claimed in claim 4,
2 wherein a first resistance between the first bit line
3 contact and the bit line contact of the first pair of
4 memory cells is detected by turning on the first
5 transistor, and a second resistance between the second
6 bit line contact and the bit line contact of the second
7 pair of memory cells is detected by turning on the second
8 transistor.

1 7. A method for detecting alignment of deep trench
2 capacitors and word lines in DRAM devices, comprising:

3 providing a wafer with at least one scribe line
4 region and at least one memory region;
5 forming a plurality of pairs of memory cells in the
6 memory region and at least one test device in
7 the scribe line simultaneously, wherein each
8 pair of memory cells includes an active area,
9 two deep trench capacitors deposited at two ends
10 of the active area, two word lines disposed
11 above the active area, and a bit line contact
12 disposed between the two word lines and
13 electrically coupled to the active area, the
14 test device including:
15 parallel first and second bar-type deep
16 trenches capacitors disposed in the scribe
17 line region; wherein the first and second
18 bar-type deep trenches capacitors extend
19 to the first and second pairs of memory
20 cells adjacent to the first active area
21 respectively, and electrically coupled to
22 bit line contacts of the first and second
23 pairs of memory cells respectively;
24 a first transistor having a source coupled to
25 the first bar-type deep trench capacitor;
26 a second transistor having a source coupled to
27 the second bar-type deep trench capacitor;
28 and
29 a first bit line contact electrically coupled
30 to drains of the first and second
31 transistors;

32 measuring a first resistance between the first bit
33 line contact and the bit line contact of the
34 first pair of memory cells and a second
35 resistance between the second bit line contact
36 and the bit line contact of the second pair of
37 memory cell; and
38 determining alignment of the deep trench capacitors
39 and word lines in the memory regions according
40 to alignment of the first and second
41 resistance.

1 8. The method as claimed in Claim 7, wherein two
2 word lines are disposed on two sides of the first bit
3 line contact respectively, as gates of the first and the
4 second transistors respectively.

1 9. The method as claimed in Claim 8, further
2 comprising:
3 determining alignment of the first and second bar-
4 type deep trenches capacitors and two word
5 lines of the test device according to the first
6 resistance and the second resistance; and
7 determining alignment of the deep trench capacitors
8 and word lines in the memory regions according
9 to alignment of the first and second bar-type
10 deep trenches capacitors and two word lines of
11 the test device.